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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,069	10/14/2003	Shlomo Novotny	2442/142	4368

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EXAMINER	
TA, THO DAC	

ART UNIT	PAPER NUMBER
2833	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/685,069	NOVOTNY ET AL.
	Examiner	Art Unit
	Tho D. Ta	2833

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-17,19-24,26-31 and 33-37* is/are rejected.

7)☒ Claim(s) *6,7,18,25 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 8-16, 19-24, 26-31, 33-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Searls et al. (6,752,635).

In regard to claim 1, Searls et al. discloses a socket 204 for forming electrical connections between a first surface 202 having a first contact array 209, 248 and a second surface 208 having a second contact array 216, 246, the socket 204 comprising: a plate having a thickness, the plate including surfaces defining a plurality of passages 212, 244 extending through the thickness of the plate; and a plurality of compliant contacts 106, 206, each contact inserted into one of the passages 212, 244, each contact including a first contact surface 118, 240 for electrically engaging the first contact array and a second contact surface 114, 238 for electrically engaging the second contact array, wherein at least one (106) of the contacts 106, 206 is a low current contact, and at least one (206) of the contacts 106, 206 is a high current contact capable of passing more current than the low current contact.

In regard to claim 2, Searls et al. discloses that the high current contact 206 is larger than the low current contact 106.

In regard to claim 3, Searls et al. discloses that the high current contact 206 is at least twice as big as the low current contact 106.

In regard to claim 4, Searls et al. discloses that the plurality of contacts 106, 206 form an array having an outer periphery, the high current contact 206 positioned on the outer periphery (see fig. 2B).

In regard to claim 5, Searls et al. discloses that the high current contact 206 at least partially shields one or more contacts 106 positioned within the array from electromagnetic interference (see fig. 2B).

In regard to claim 8, Searls et al. discloses that the high current contact 206 varies in shape from the at least one low current contact 106 so as to provide alignment information.

In regard to claim 9, Searls et al. discloses that the plate 204 is made from a single piece of insulating material.

In regard to claim 10, Searls et al. discloses that a frame (perimeter wall in fig. 2B) attached to the plate 204.

In regard to claim 11, Searls et al. discloses that at least one of the first contact array 209, 248 and second contact array 216, 246 is one of a land grid array and a ball grid array.

In regard to claim 12, Searls et al. discloses a socket assembly comprising: a first surface 208 including a first contact array 209, 248; a second surface 202 including a second contact array 216, 246; and a socket 204, wherein the first contact surface 118, 240 of each contact 106, 206 is electrically coupled to the first contact array 209, 248, and the second contact surface 114, 238 of each contact 106, 206 is electrically coupled to the second contact array 216, 246.

In regard to claim 13, Searls et al. discloses that the first surface 208 is of an integrated circuit and the second surface 202 is of a circuit board.

In regard to claim 14, Searls et al. discloses that the second surface 202 is a circuit board.

Although the prior art does not specifically disclosed the claimed capacitor and resistor is positioned between the array socket and the circuit board, these features are seen to be an inherent teaching of that device since a LGA socket for providing a

current between the PCB and the integrated circuit is disclosed and it is apparent that some type of capacitor and resistor must be present for the LGA socket assembly to function as intended.

In regard to claim 15, Searls et al. discloses a method of passing signals between a first surface 208 having a first contact array 209, 248 and a second surface 202 having a second contact array 216, 246, the method comprising: providing a socket 204 having a plurality of compliant contacts 106, 206, wherein at least one of the contacts 106, 206 is a low current contact (106) and at least one of the contacts 106, 206 is a high current contact (206); compressing the socket 204 between the first surface 208 and the second surface 202, such that a first contact surface 118, 240 of each contact 106, 206 is electrically coupled to the first contact array 209, 248, and a second contact surface 114, 238 of each contact 106, 206 is electrically coupled to the second contact array 216, 246, passing a current through the high current contact 206, the current greater than a maximum current that can be passed through the low current contact 106.

In regard to claim 16, Searls et al. discloses that the second surface 202 is a circuit board. Although the prior art does not specifically disclosed the claimed capacitor and resistor is positioned between the array socket and the circuit board, these features are seen to be an inherent teaching of that device since a LGA socket for providing a current between the PCB and the integrated circuit is disclosed and it is apparent that

some type of capacitor and resistor must be present for the LGA socket assembly to function as intended.

In regard to claim 19, Searls et al. discloses that the high current contact 206 at least partially shields one or more contacts 106 positioned within the array from electromagnetic interference (see fig. 2B).

In regard to claim 20, Searls et al. discloses that at least one of the first contact array 209, 248 and second contact array 216, 246 is one of a land grid array and a ball grid array.

In regard to claim 21, Searls et al. discloses a socket for forming electrical connections between a first surface 208 having a first contact array 209, 248 and a second surface 202 having a second contact array 216, 246, the socket 204 comprising: a plate having a thickness, the plate including surfaces defining a plurality of passages 212, 244 extending through the thickness of the plate; and a plurality of compliant contacts 106, 206, each contact 106, 206 inserted into one of the passages 212, 214, each contact 106, 206 including a first contact surface 118, 240 for electrically engaging the first contact array 209, 248 and a second contact surface 114, 238 for electrically engaging the second contact array 216, 246, wherein at least one of the contacts 106, 206 is a small contact (106) and at least one of the contacts 106, 206 is a large contact (206), the large contact 206 at least twice as big in size as the

small contact 106.

In regard to claim 22, Searls et al. discloses that the large contact 206 is capable of passing more current than the small contact 106.

In regard to claim 23, Searls et al. discloses that the plurality of contacts 106, 206 form an array having an outer periphery, the high current contact 206 positioned on the outer periphery (see fig. 2B).

In regard to claim 24, Searls et al. discloses that the high current contact 206 at least partially shields one or more contacts 106 positioned within the array from electromagnetic interference (see fig. 2B).

In regard to claim 26, Searls et al. discloses that at least one of the first contact array 209, 248 and second contact array 216, 246 is one of a land grid array and a ball grid array.

In regard to claim 27, Searls et al. discloses a socket assembly comprising: a first surface 208 including a first contact array 209, 248; a second surface 202 including a second contact array 216, 246; and a socket 204, wherein the first contact surface 118, 240 of each contact 106, 206 is electrically coupled to the first contact

array 209, 248, and the second contact surface 114, 238 of each contact 106, 206 is electrically coupled to the second contact array 216, 246.

In regard to claims 28, 29, Searls et al. discloses that the second surface 202 is a circuit board. Although the prior art does not specifically disclosed the claimed electronic component is positioned between the array socket and the circuit board, these features are seen to be an inherent teaching of that device since a LGA socket for providing a current between the PCB and the integrated circuit is disclosed and it is apparent that some type of electronic component such as capacitor and resistor must be present for the LGA socket assembly to function as intended.

In regard to claim 30, Searls et al. discloses a method of passing signals between a first surface 208 having a first contact array 209, 248 and a second surface 202 having a second contact array 216, 246, the method comprising: providing a socket 204 having a plurality of compliant contacts 106, 206, wherein at least one of the contacts 106, 206 is a small contact and at least one of the contacts 106, 206 is a large contact, the large contact 206 twice as big in size as the small contact 106; compressing the socket 204 between the first surface 208 and the second surface 202, such that a first contact surface 118, 240 of each contact 106, 206 is electrically coupled to the first contact array 209, 248, and a second contact surface 114, 238 of each contact 106, 206 is electrically coupled to the second contact array 216, 246.

In regard to claim 31, Searls et al. discloses the step of passing a current through the large contact 206, the current greater than a maximum current that can be passed through the small contact 106.

In regard to claim 33, Searls et al. discloses the step of using the large contact 206 to shield at least one of the plurality of contacts 106 from electromagnetic interference.

In regard to claim 34, Searls et al. discloses that the second surface 202 is a circuit board. Although the prior art does not specifically disclosed the claimed electronic component is positioned between the array socket and the circuit board, these features are seen to be an inherent teaching of that device since a LGA socket for providing a current between the PCB and the integrated circuit is disclosed and it is apparent that some type of electronic component such as capacitor and resistor must be present for the LGA socket assembly to function as intended.

In regard to claim 35, Searls et al. discloses a plate for a socket 204, the socket 204 including a plurality of double sided contacts 106, 206 for forming electrical connections between a first surface 208, 202 having a first contact array 209, 248 and a second surface 202 having a second contact array 216, 246, the plate having a thickness, the plate comprising: surfaces defining an array of passages 212, 244, each passage 212, 244 extending through the thickness of the plate such that one of the

contacts 106, 206 can be inserted into each passage 212, 244, wherein at least one of the passages 212, 244 is a small passage 212 having a first size, and at least one of the passages 212, 244 is a large passage 244 having a second size larger than the first size, the large passage 244 capable of having a larger contact 206 inserted compared to the small passage 212.

In regard to claim 36, Searls et al. discloses the large passage 244 forms a rectangle extending the length of at least two or more small passages 212.

In regard to claim 37, Searls et al. discloses that the array has an outer periphery, the large passage 244 positioned on the outer periphery.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Searls et al.

In regard to claim 17, Searls et al. is silent about connecting the high current contact 206 to one of a ground signal or a power signal. Official Notice is taken that both the concept and the advantages of connecting electrical contact to one of a ground signal or a power signal are well known and expected in the art.

Allowable Subject Matter

5. Claims 6, 7, 18, 25 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: In regard to claims 7, 18, 25, 32, the prior art fails to provide, teach or suggest the high current contact acts as a spacer. In regard to claim 6, the prior art fails to provide, teach or suggest the array is a rectangular array having four sides, and wherein one or more high current contacts are positioned on each side of the rectangular array.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tho D. Ta whose telephone number is (571) 272-2014. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula A. Bradley can be reached on (571) 272-2800 ext 33. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

THO D. TA
PRIMARY EXAMINER

tdt
09/23/04